ESDi

PRIMARIUS

Chip-level HBM Analysis Platform

Introduction

ESDi platform covers a comprehensive suite of advanced full-chip ESD (Electrostatic Discharge) network verification tools, including a schematic-based HBM checker ESDi-SC, a chip-level HBM checker ESDi, and ESDi-XL, and chip-level HBM analysis tool for multi-threaded simulation.

ESDi platform ensures accurate simulation of HBM discharge paths, providing accuracy and speed with non-linear simulation technology and TLP models. This suite facilitates layout extraction, identifies pads and ESD protection devices, and generates reduced-order models for parasitic layout resistances. Chip-level verification is performed by simulating pad-to-pad HBM strikes, mapping IR-drops, and calculating current densities and stress conditions of devices.

ESDi platform excels in identifying overstressed internal-circuit devices, incorrect or missing ESD cells, excessive voltages developed on pads due to HBM stress, EM (electro-migration) issues due to undersized interconnects (metals or vias), high bus resistances leading to excessive voltage stress over protected devices, and imbalanced current distribution over the fingers inside ESD devices to avoid yield and reliability issues.

ESDi platform has been recognized by industry-leading chip design houses and manufacturers, providing comprehensive HBM verification solutions at various stages of the design process.

ESDi-SC
Schematic-based HBM verification

ESDi
Chip-level layout-based HBM verification

ESDi-XL
Multi-threaded layout & schematic -based HBM verification

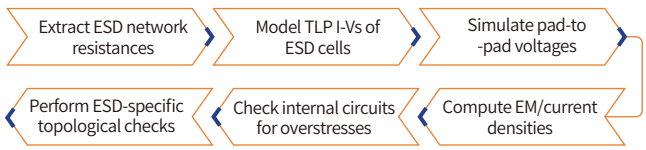
Features

- Adopts ESD cell I-V data and extracted resistances to compute pad-to-pad voltages developed during ESD testing
- Checks internal circuits for voltage and current stress developed due to excessive pad-to-pad voltages
- ESD-specific rule-based topological checks for comprehensive internal circuit protection design
- Computes current densities in interconnects, and displays them in a field-view GUI
- Supports AGF & SVDB based mapping between layout and schematics of third-party tools for higher accuracy
- Multi-threaded and efficient solver to ensure quick results

Key Advantages

- Comprehensive
  Covers all phases of the design flow: schematics-only and post-layout
- Leading
  Covers metalization and internal circuit sneak-path checks to highlight marginal devices, avoiding costly field failures in marginal designs
- Accurate
  Simulation based approach ensures the highest level of accuracy
- Systematic
  ESD sign-off verification flow before tape out with comprehensive coverage of all HBM-stress conditions, including complex multi-power domain designs
- Cost-effective
  Low cost set up and high engineering productivity designed to be useful in all stages of the design flow, from inception to final tapeout

ESD Network and Internal Circuits Check Flow

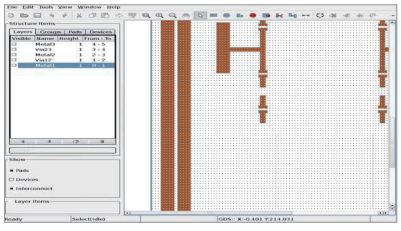


Applications

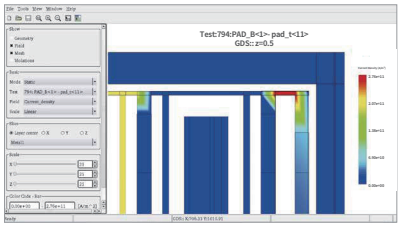
- HBM analysis for Analog and Mixed Signal chips
- HBM analysis for automotive chips
- HBM analysis for PMICs
- HBM analysis for digital chips

Application Examples

Layout-Based Analysis



Current Densities & Voltages Analysis



Chip-level ESD-network Verification

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